

Timing diagram for a 6-bit shift register. The top signal is DATA\_T, which is 1 for bit 1, 0 for bit 2, 1 for bit 3, 0 for bit 4, 1 for bit 5, and 0 for bit 6. Below it are five clock signals, CKL1 through CKL5, each with a period of 1 unit. The shift register outputs are shown as a sequence of bits: 1, 0, 1, 0, 1, 0. An arrow points to the output of the 5th stage (bit 1) with the text "throw away the extra bit".

FIG. 4

# Replacement sheet

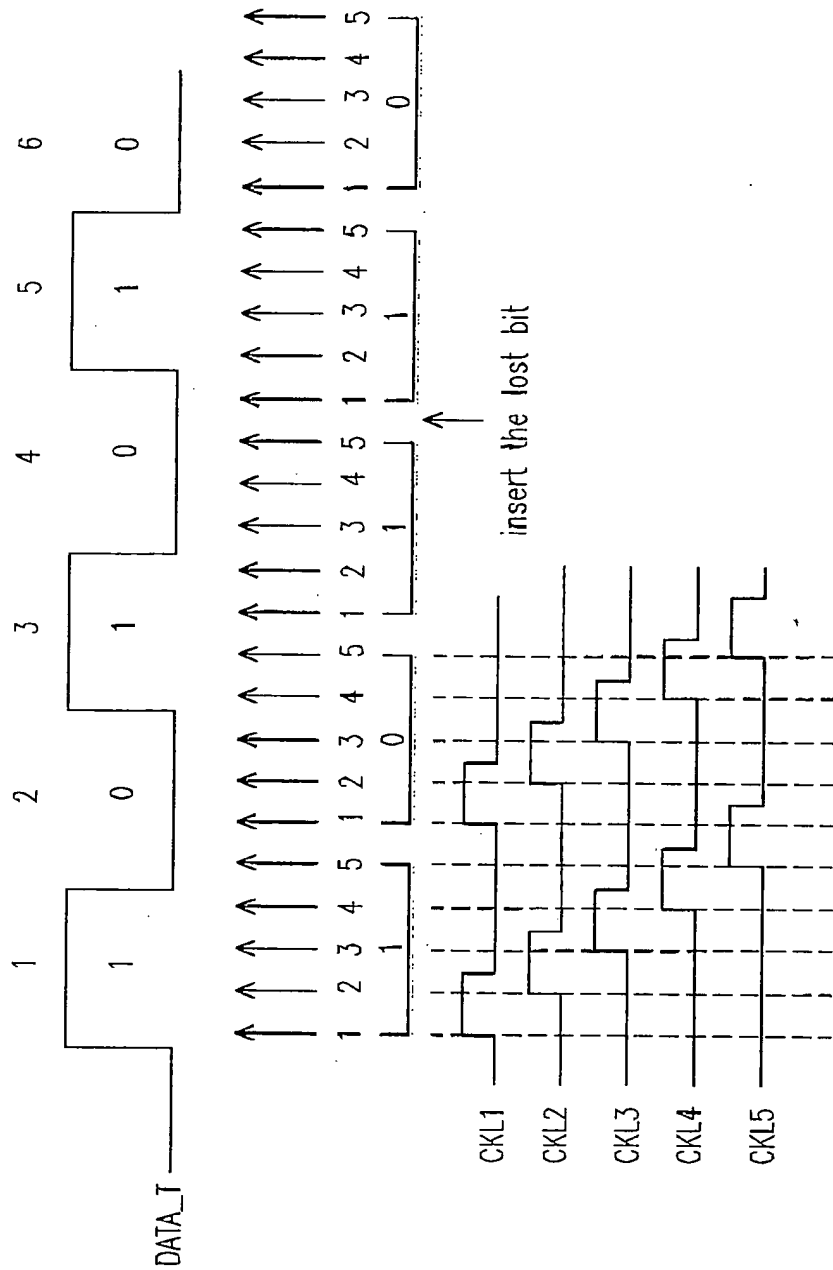


FIG. 6